에이디반도체

TS01S

1-Ch Differential Sensitivity Calibration Capacitive Touch Sensor

SPECIFICATION V3.0

November 2011

AD Semiconductor

■ Revision History

Rev.	Description of change	Date	Originator
1.0	First creation	07.08.24	KD PARK
2.0	Three sensitivity step	07.09.19	KD PARK
2.1	8.2 Marking Description Device code S1 => S	07.11.12	KD PARK
2.2	1.1 General Feature, Low power consumption	07.12.06	KD PARK
2.3	ESD Level modification, Note3 addition	08.01.19	KD PARK
2.4	ESD Level modification, Note3 removal	08.02.27	KD PARK
2.5	Operating current addition	10.08.17	KD PARK
2.6	Current consumption modification	10.11.15	KD PARK
2.7	Sensitivity Option modification	11.06.27	KD PARK
2.8	Reset Voltage modification, Revision History Page addition	11.12.15	HS KWAK
2.9	Reset Voltage Min/Max addition, reset operation caution addition Current consumption modification	12.01.12 12.02.21	HS KWAK KD PARK
3.0	Current consumption modification	12.02.21	KD PARK

1 Specification

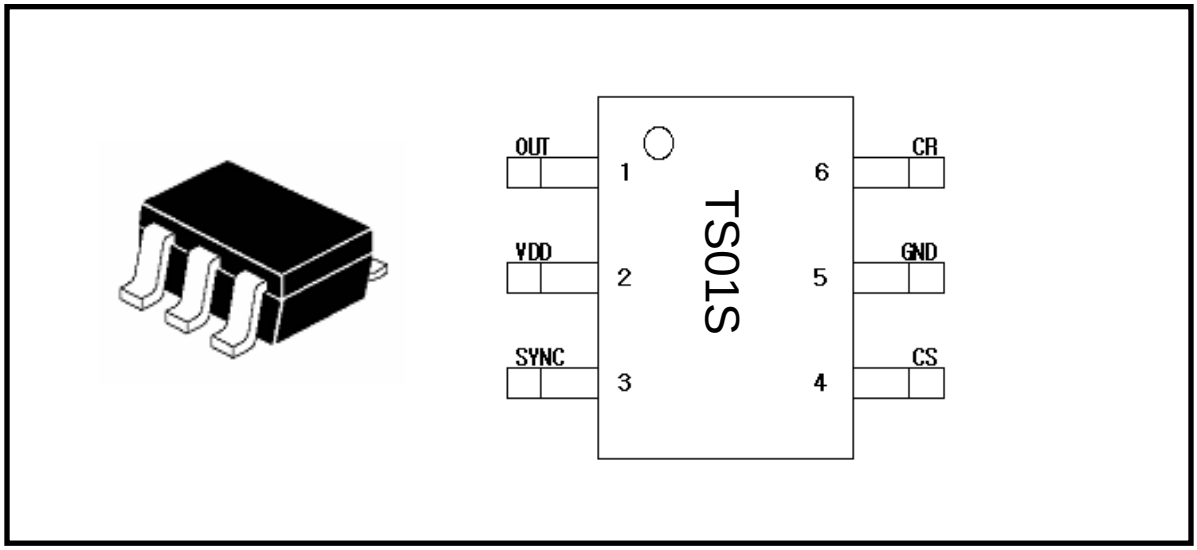
1.1 General features

- 1-Channel capacitive touch sensor with differential sensitivity calibration
- Low power consumption
- Uniformly adjustable sensitivity
- Sync function for parallel operation
- Three steps sensitivity available without external component
- Open-drain digital output
- Internal power on reset
- Embedded common and normal noise elimination circuit
- RoHS compliant SOT-26 package

1.2 Application

- Home appliance
- Mobile application (PMP, Navigation, MP3 etc)
- Membrane switch replacement
- Human interface for toys & interactive games
- Sealed control panels, keypads

1.3 Package (SOT-26)



TS01S SOT-26 (Drawings not to scale)

2 Pin Description (SOT-26)

PIN Number	Name	I/O	Description	Protection
1	OUTPUT	Digital Output	Touch detect output	VDD/GND
2	VDD	Power	Power (2.5V ~ 5.0V)	GND
3	SYNC	Analog Input/Output	Self operation signal output Peripheral operation signal input Sensitivity selection input [Note1]	VDD/GND
4	CS	Analog Input	Capacitive sensor input	VDD/GND
5	GND	Ground	Supply ground	VDD
6	CR	Analog Input	Reference capacitive sensor input for differential sensitivity calibration	VDD/GND

Note1 : Refer to chapter 6.3, 6.4 SYNC implementation

3 Absolute Maximum Rating

Supply voltage	5.5 V
Maximum voltage on any pin	VDD+0.3 V
Maximum current on any PAD	100mA
Continuous power Dissipation	200mW
Storage Temperature	−50 ~ 150℃
Operating Temperature	−20 ~ 75℃
Junction Temperature	150℃

Note2 : Unless any other command is noted, all above are operated in normal temperature.

4 ESD & Latch-up Characteristics

4.1 ESD characteristics

Mode	Polarity	Minimum Level	Reference
H.B.M	Pos / Neg	8000V	VDD
		8000V	VSS
		8000V	P to P
M.M	Pos / Neg	500V	VDD
		500V	VSS
		500V	P to P
C.D.M	Pos / Neg	800V	DIRECT

4.2 Latch-up characteristics

Mode	Polarity	Minimum Level	Test Step
I Test	Positive	25mA ~ 100mA	25mA
	Negative	−25mA ~ −100mA	
V supply over 5.0V	Positive	1V ~ 7.5V	0.5V

5 Electrical Characteristics

▪ V_{DD}=3.3V (Unless otherwise noted), T_A = 25℃

Characteristics	Symbol	Test Condition	Min	Typ	Max	Units
Operating supply voltage	V_{DD}		2.5	3.3	5.0	V
Current consumption	I_{DD}	V_{DD}= 3.3V	–	140	210	μA
		V_{DD}= 5.0V	–	200	280	
Output maximum sink current	I_{OUT}	T_A = 25℃	–	–	4.0	mA
Internal reset voltage	V_{DD_RST}	T_A = 25℃	1.2	1.76	2.2	V
Sense input capacitance range [Note3]	C_S		–	10	100	pF
Reference input capacitance range [Note4]	C_R		–	12	100	Ω
Sense input resistance range	R_S		–	200	1000	
Minimum detectable capacitance variation	ΔC_S	C_S = 10pF	0.2	–	–	pF
Output impedance (open drain)	Zo	ΔC_S > 0.2pF	–	12	–	Ω
Self calibration time after V_{DD} setting	T_{CAL}	ΔC_S < 0.2pF	–	30M	–	ms
			–	200	–	
Maximum supply voltage rising time	T_{R_VDD}		–	–	100	ms
Recommended sync resistance range	R_{SYNC}		1	2	20	MΩ

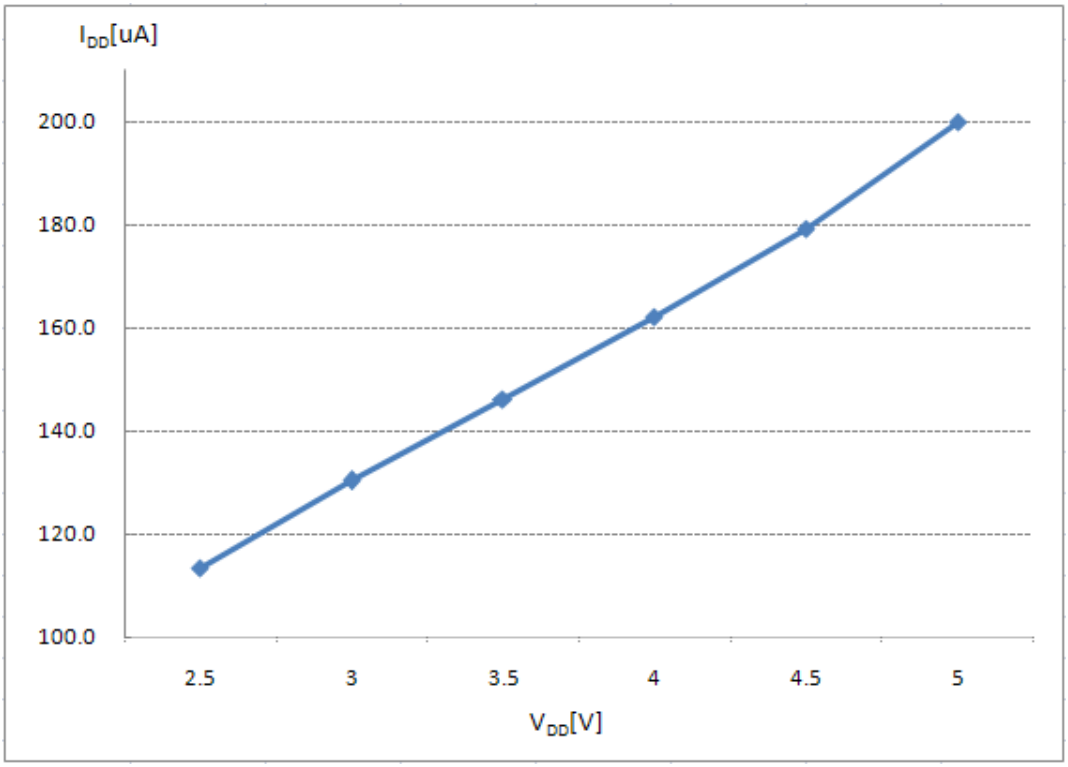
Note 3: The sensitivity can be increased with lower C_S value.
The recommended value of C_S is 10pF when using 3T PC(Poly Carbonate) cover and 10 ㎜ x 7 ㎜ touch pattern and middle sensitivity selection.

Note 4: C_R value is recommended as same that of C_{S_TOT} as possible for effective differential sensitivity calibration. $C_{S\_TOT} = C_S + C_{PARA}$ (C_{PARA} is parasitic capacitance of CS pin)
If proper CR capacitor value is used, CR pin has almost same frequency as that of CS pin.

6 TS01S Implementation

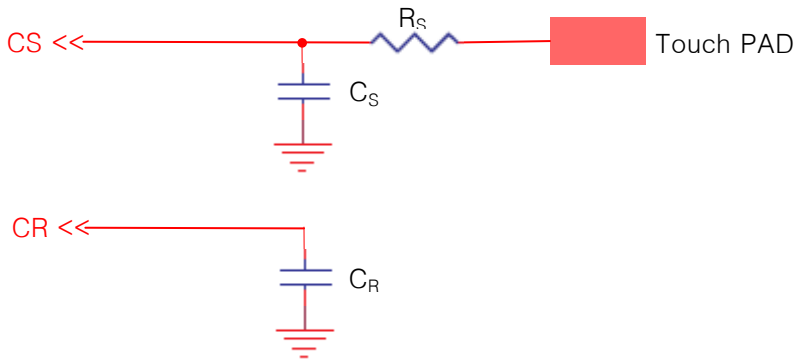
6.1 Current consumption

TS01S uses internal bias circuit, so internal clock frequency and current consumption is not adjusted. The typical current consumption curve of TS01S is represented in accordance with V_{DD} voltage as below. The higher V_{DD} requires more current consumption.
Internal bias circuit can make the circuit design simple and reduce external components.

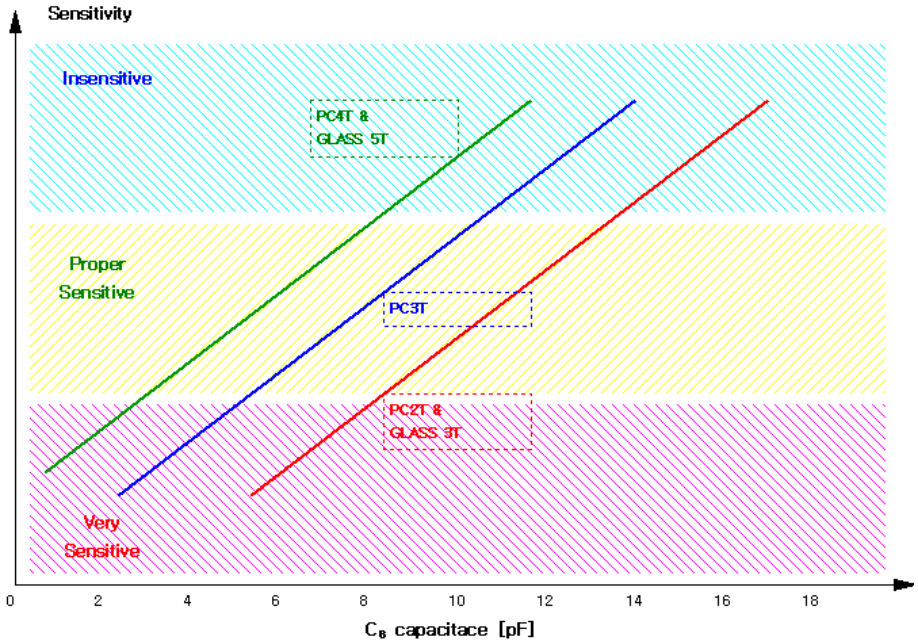


Typical current consumption curve of TS01S

6.2 CS and CR implementation



The parallel capacitor C_S is added to CS and C_R to CR to adjust fine sensitivity. The major factor of the sensitivity is C_S. The sensitivity would be increased when smaller C_S value is used. (Ref. below Sensitivity Example Figure) The C_R value should be almost the same as the total CS capacitance (C_{S_TOT}) for effective differential sensitivity calibration. The total CS capacitance is composed of C_S which is set for optimal sensitivity and parasitic capacitance of CS pattern (C_{PARA}). The parasitic capacitance of CS pattern is about 2pF if normal touch pattern size is used. But in the case of using larger touch pattern, C_{PARA} is bigger than normal value.
The R_S is serial connection resistor to avoid malfunction from external surge and ESD. (It might be optional.) From 200Ω to 1kΩ is recommended for R_S. The size and shape of touch PAD might have influence on the sensitivity. The sensitivity will be optimal when the size of PAD is approximately an half of the first knuckle (it's about 10 ㎜ x 7 ㎜). The connection line of CS to the touch PAD is recommended to be routed as short as possible to prevent from abnormal touch detection caused by connection line.

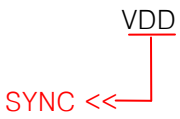


Sensitivity example figure of TS01S (when normal sensitivity selection selected)

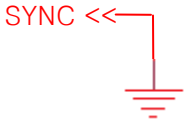
6.3 SYNC implementation

From two TS01S to ten TS01S (or other TS series touch sensor) can work on the one application at the same time thanks to SYNC function with this pin. The SYNC pulse prevents over two sensing signal from interfering with each other. During the sense disenable period and SYNC input becomes high, internal clock is suspended. The R_{SYNC} is pull-down resistor of SYNC pin. Too big value of R_{SYNC} makes the SYNC pulse falling delay, and too small value of R_{SYNC} makes rising delay. The typical value of R_{SYNC} is 2MΩ.
TS01S has high sensitivity when SYNC is implemented as above figure (connect R_{SYNC} between SYNC and GND).

6.4 SYNC implementation for sensitivity selection.



Sync connection for low sensitivity

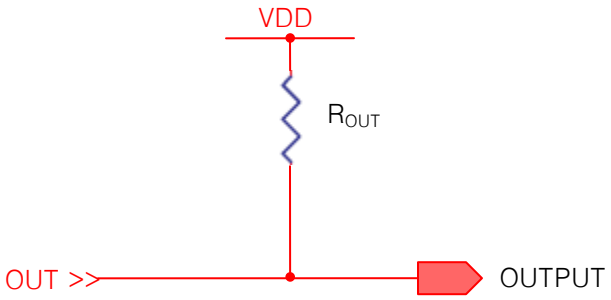


Sync connection for high sensitivity

Another function of SYNC pin of TS01S is the selection of sensitivity without any additional external component. The SYNC implementation for sensitivity selection is informed as below chart.

SYNC Connection	Using R_{SYNC} Connection	Connected to VDD	Connected to GND
Sensitivity	Middle	Low	High

6.5 OUTPUT implementation



The OUT is an open drain structure. For this reason, the connection of pull-up resistor R_{OUT} is required between OUT and VDD or another lower voltage node. When R_{OUT} is connected to higher voltage node than VDD, the output current passes through protection diode to VDD and abnormal operation may be occurred.
The maximum output sink current is 4mA, so over a few kΩ must be used as R_{OUT}. Normally 10kΩ is used as R_{OUT}. The OUT is high in normal situation, and the value is low when a touch is detected on CS.

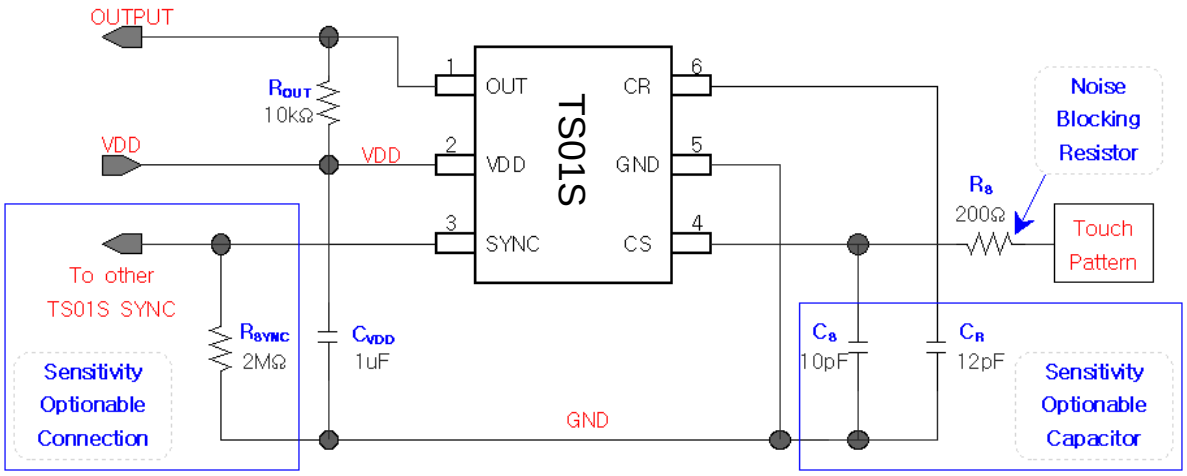
6.6 Internal reset operation

The TS01S has stable internal reset circuit that offers reset pulse to digital block. The supply voltage for a system start or restart should be under V_{DD_RST}. No external components required for TS01S power reset, thus it helps simple circuit design and minimize the cost of application.

☞ CAUTION1: The V_{DD} rising time should be less then 100ms for proper power on reset.
☞ CAUTION2: If the supply voltage dropped under the V_{DD_RST}(for some reason), the supply voltage must keep under the V_{DD_RST} at least 5us(for proper power on reset).

7 Recommended Circuit Diagram

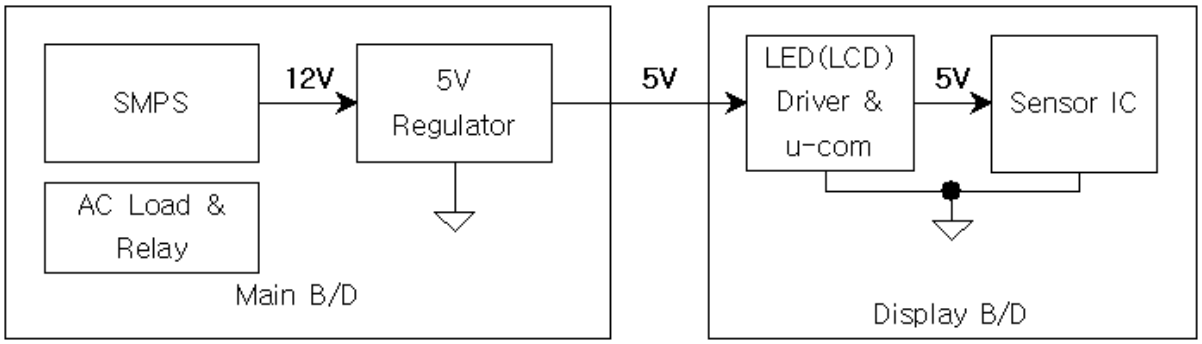
7.1 Apllication Example



- The capacitor and resistor might be connected with CS (pin4) for getting a stable sensitivity.
- The capacitor value which is connected to CR pin (C_R) should be almost the same as the total CS capacitance (include parasitic capacitance) for an effective differential sensitivity calibration.
- TS01S is reset by internal reset circuit. VDD voltage rising time should be shorter than 100msec for proper operation.
- The sensitivity can be adjusted through a connection of SYNC pin. (Refer to chapter 6.4)
- From two TS01S to ten TS01S (or other TS series touch sensor) can work on the one application at the same time thanks to SYNC function. (Refer to chapter 6.3)
- TS01S OUT port has an open drain structure. The pull-up resistor should therefore be needed as above figure.
- VDD periodic voltage ripples over 50mV or the ripple frequency which is lower than 10 kHz it can cause wrong sensitivity calibration. To prevent above problem, power (VDD, GND) line of touch circuit should be separated from the other circuit. Especially the LED driver power line or digital switching circuit power line should be certainly treated to be separated from touch circuit.
- The C_S pattern should be routed as short as possible and the width of the line should be around 0.25mm.
- The C_S pattern routing should be formed by bottom metal (opposite metal of touch PAD).
- The capacitor which is between VDD and GND is an obligation. It should be placed as close as possible from TS01S.
- The empty space of PCB must be filled with GND pattern to strengthen GND pattern and to prevent external noise that causes interference with the sensing frequency.

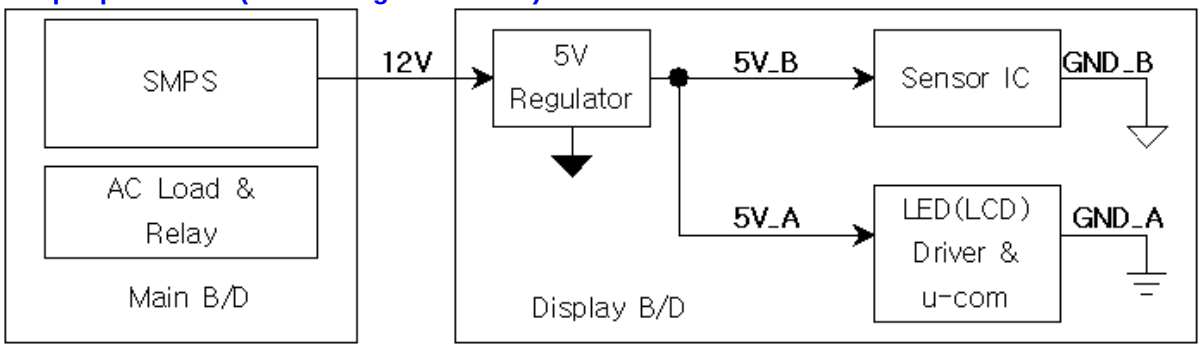
7.2 Example – Power Line Split Strategy

A. Not split power line (Bad power line design)

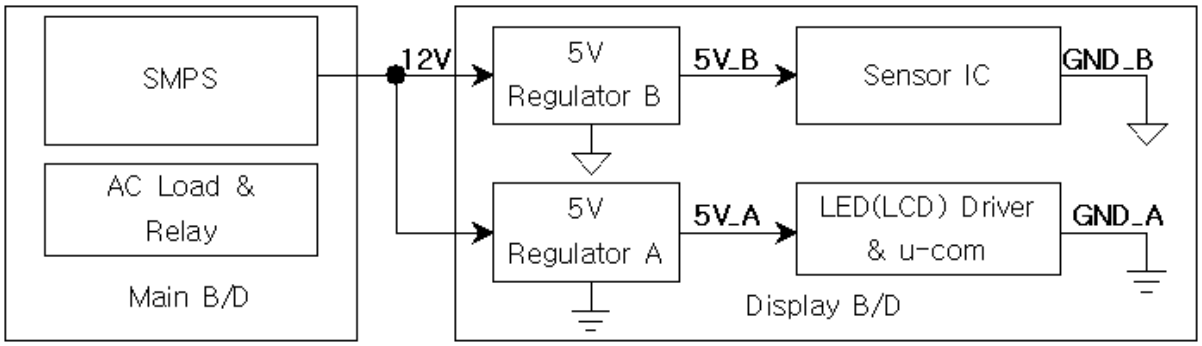


- The noise that is generated by AC load or relay can be loaded at VDD power line.
- A big inductance might be appeared in case of the connection line between main board and display board is too long, moreover the voltage ripple could be generated by LED (LCD) display driver at VDD.

B. Split power line (One 5V regulator used) – Recommended

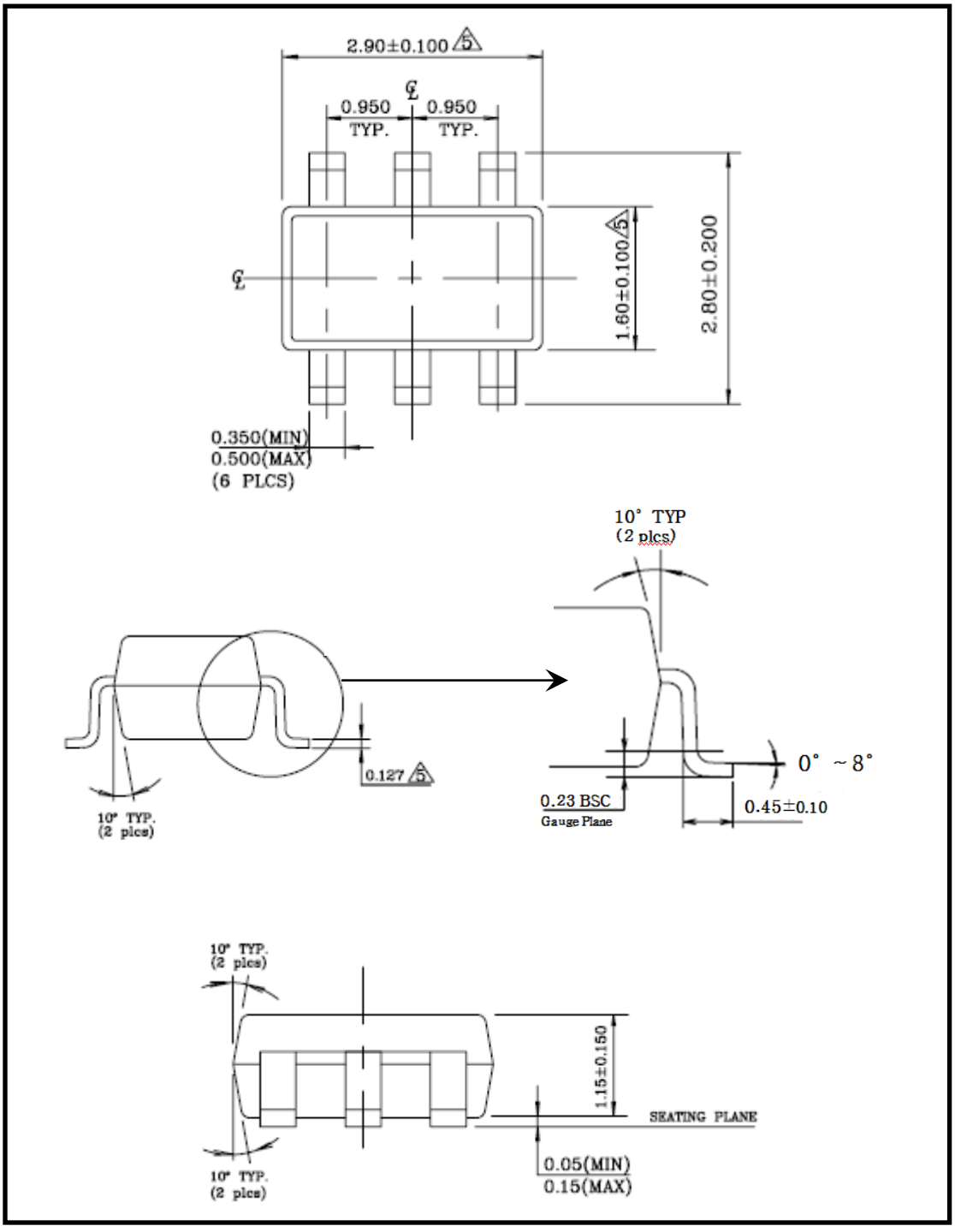


C. Split power line (Separated 5V regulator used) – Strongly recommended



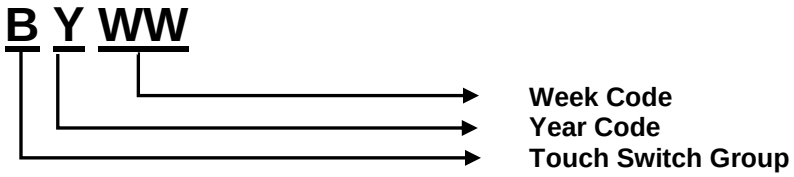
8 PACKAGE DESCRIPTION

8.1 Mechanical Drawing



NOTE:
1. Dimensions and tolerances are as per ANSI Y14.5, 1982.
2. Package surface to be matte finish VDI 11 ~ 13.
3. Die is facing up for mold. Die is facing down for trim/form, ie. Reverse trim/form.
4. The footlength measuring is based on the gauge plane method.
5. Dimension is exclusive of mold flash and gate burr.
6. Dimension is exclusive of solder plating.
7. All dimensions are mm.

8.2 Marking Description



Year Code	P	R	S	T	U	V	W	X	Y	Z
Production Year	2007	2008	2009	2010	2011	2012	2013	2014	2015	2016

NOTES:

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